MSCA83S - 86KX2 (128MB 140-Pin SDRAM Module)

DESCRIPTION

The MSCA83S-86KX2 is 16M bit x 64 Synchronous Dynamic RAM high density memory module. The MSCA83S-86KX2 consists of eight CMOS 8Mx16 bit with 4banks Synchronous DRAMs in TinyBGA package on a 140-Pin glass-epoxy substrate. Two 0.1uf decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The MSCA83S-86KX2 is a Memory Module and is intended for mounting into 140-Pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies , programmable latencies allows the same device to be useful for a variety of high bandwidth , high performance memory system application.

FEATURES

- Performance range - 100MHz (Max Freq.)(CL=2)
- Burst mode operation
- Auto & self refresh capability (4096 Cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
- Latency (Access from column address)
- Burst length (1 , 2 , 4 , 8 & Full page)
- Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- PCB : Height (1575 mil) , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	GND	2	GND	49	DQ24	50	DQ8	97	VDD	98	VDD
3	DQ16	4	DQ0	51	DQ25	52	DQ9	99	NC	100	NC
5	DQ17	6	DQ1	53	DQ26	54	DQ10	101	NC	102	NC
7	DQ18	8	DQ2	55	DQ27	56	DQ11	103	NC	104	NC
9	DQ19	10	DQ3	57	GND	58	GND	105	GND	106	GND
11	VDD	12	VDD	59	DQ28	60	DQ12	107	A7	108	A6
13	DQ20	14	DQ4	61	DQ29	62	DQ13	109	BA0	110	A8
15	DQ21	16	DQ5	63	DQ30	64	DQ14	111	BA1	112	A9
17	DQ22	18	DQ6	65	DQ31	66	DQ15	113	A11	114	A10
19	DQ23	20	DQ7	67	GND	68	GND	115	VDD	116	VDD
21	GND	22	GND	69	DQ48	70	DQ32	117	DQ56	118	DQ40
23	DQM2	24	DQM0	71	DQ49	72	DQ33	119	DQ57	120	DQ41
25	DQM3	26	DQM1	73	DQ50	74	DQ34	121	DQ58	122	DQ42
27	A3	28	A0	75	DQ51	76	DQ35	123	DQ59	124	DQ43
29	A4	30	A1	77	VDD	78	VDD	125	GND	126	GND
31	A5	32	A2	79	DQ52	80	DQ36	127	DQ60	128	DQ44
33	GND	34	GND	81	DQ53	82	DQ37	129	DQ61	130	DQ45
35	CLK0	36	*CLK1	83	DQ54	84	DQ38	131	DQ62	132	DQ46
37	GND	38	GND	85	DQ55	86	DQ39	133	DQ63	134	DQ47
39	$\overline{CAS}$	40	$\overline{RAS}$	87	GND	88	GND	135	VDD	136	VDD
41	CKE0	42	$\overline{WE}$	89	CLK2	90	*CLK3	137	NC	138	NC
43	*CKE1	44	$\overline{CS0}$	91	GND	92	GND	139	GND	140	GND
45	NC	46	$\overline{CS1}$	93	DQM6	94	DQM4				
47	VDD	48	VDD	95	DQM7	96	DQM5				

PIN NAMES

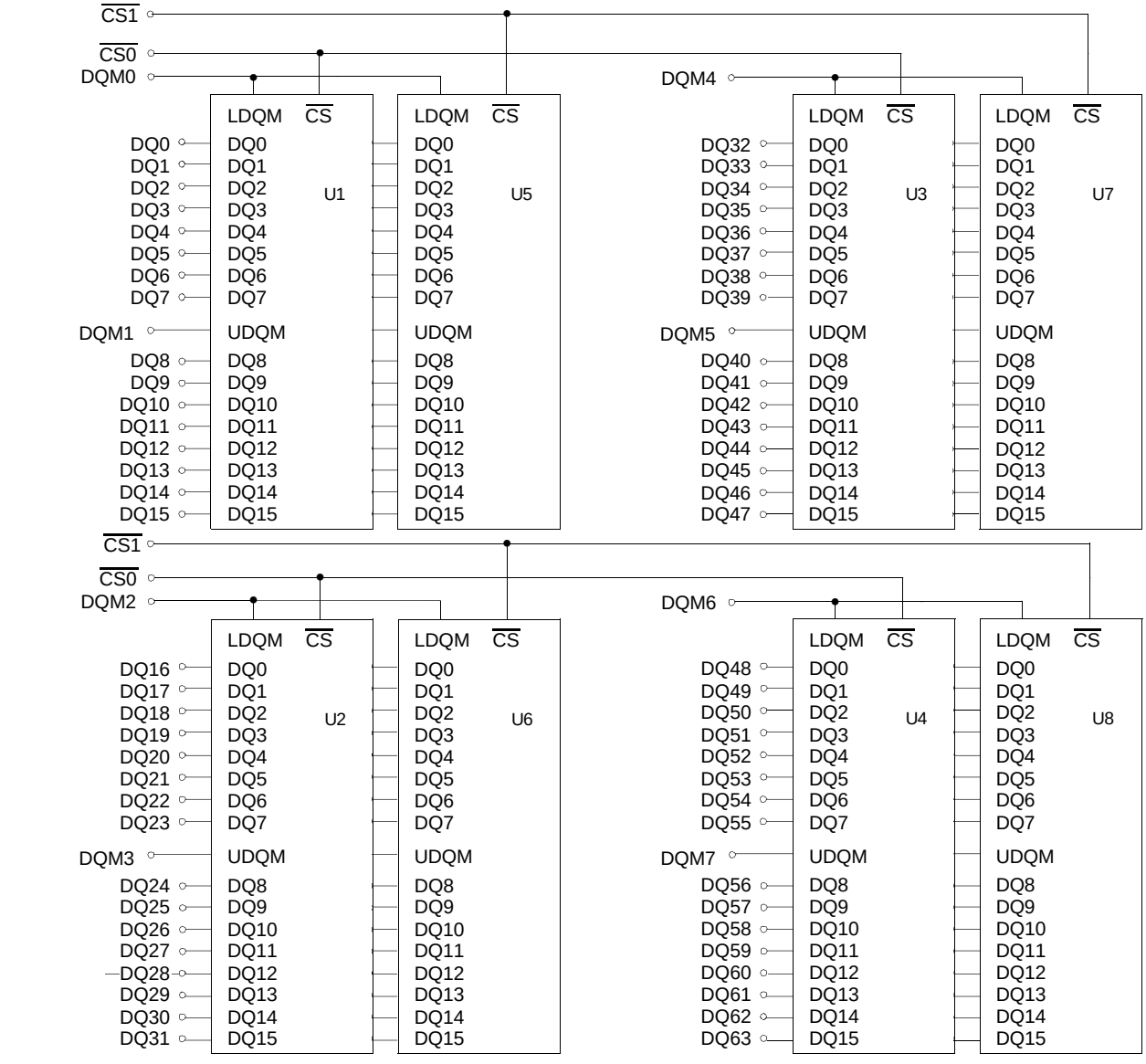
Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ,CLK2	Clock input
CKE0 ,CKE1	Clock enable input
$\overline{CS0}$, $\overline{CS1}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
NC	No connection

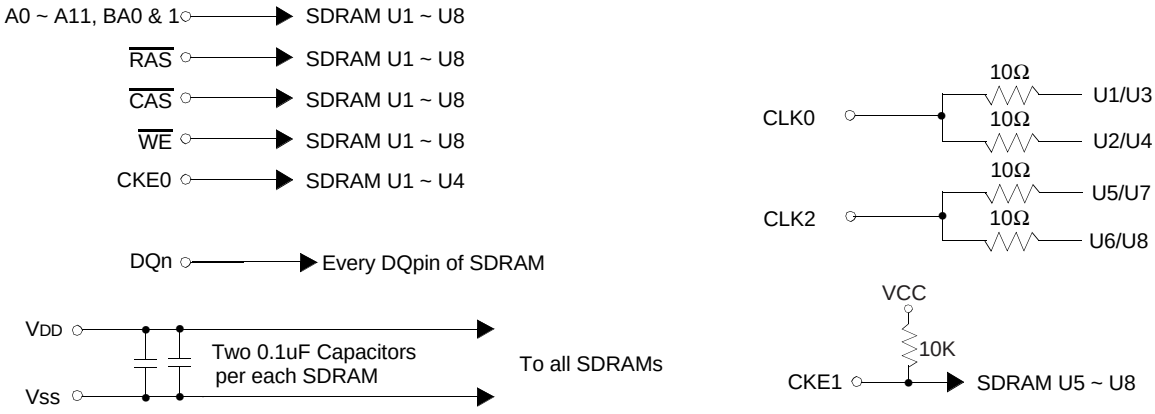
* These pins are not used in this module.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+t SS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t SHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +125	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE

(V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	22	32	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	22	32	pF
CKE (CKE0)	C_{CKE}	22	45	pF
Clock (CLK0 , CLK2)	C_{CLK}	14	20	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$)	C_{CS}	12	24	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	4	6	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	6	8	pF

DC CHARACTERISTICS

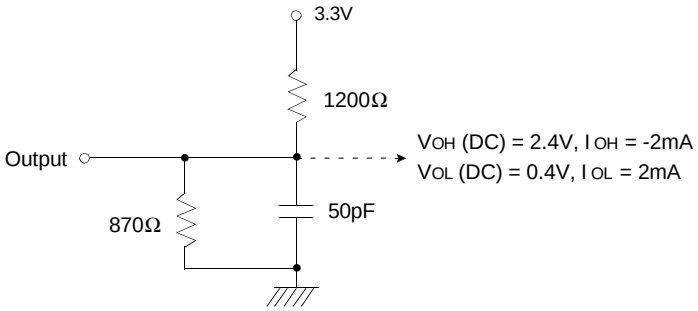
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version 128MB	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1040	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		80		
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		560	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		280	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	960	mA	1
			2	1240		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,800	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V (Low Power)		8	mA	

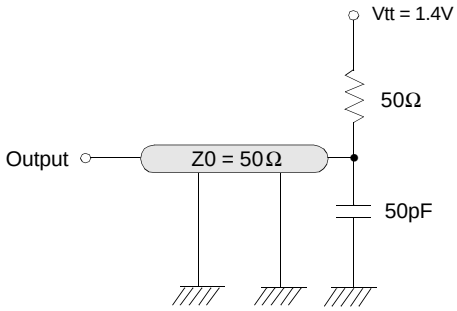
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			100 MHz		
Row active to row active delay		t_{RRD}(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	26	ns	1
Row precharge time		t_{RP}(min)	20	ns	1
Row active time		t_{RAS}(min)	50	ns	1
		t_{RAS}(max)	120	us	
Row cycle time		t_{RC}(min)	70	ns	1
Last data in to row precharge		t_{RDL}(min)	1	CLK	2
Last data in to new col. address delay		t_{CDL}(min)	1	CLK	2
Last data in to burst stop		t_{BDL}(min)	1	CLK	2
Col. address to col. address delay		t_{CCD}(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by divid ing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and re ad burst stop.

SIMPLIFIED TRUTH TABLE

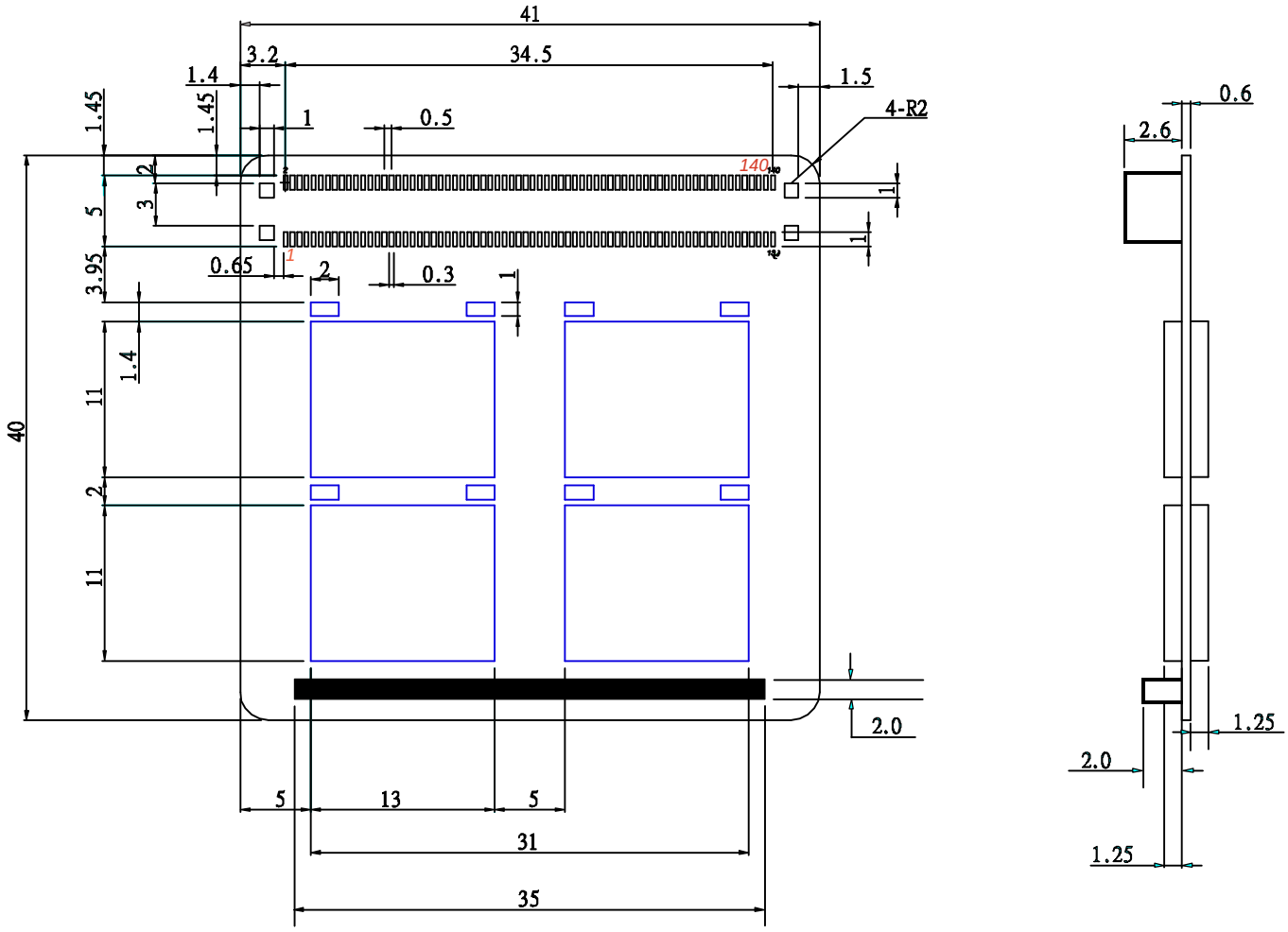
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don ′t care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ±0.005(.13) unless otherwise specified

The used device is 8Mx16bits SDRAM, TinyBGA

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